CRAY RESEARCH, INC.

CRAY-1® COMPUTER SYSTEMS

S SERIES
MAINFRAME REFERENCE MANUAL

HR-0029

MAINTENANCE CONTROL UNIT

The Maintenance Control Unit (MCU) (figure 1-3) is used for supervisory operation and maintenance on CRAY-1 models S/500 and S/1000. The MCU consists of a minicomputer, a tape drive, a removable pack disk drive, a printer/plotter, and two operator consoles. It can be used to enter jobs locally.

Figure 1-3. Maintenance Control Unit

Figure 1-6. DD-29 Disk Storage Unit

CONDENSING UNITS

Condensing units (figure 1-8) contain the major components of the refrigeration system used to cool the CRAY-1 computer chassis. Heat is removed from the condensing unit by a secondary cooling system separate from the CRAY-1 Computer System.

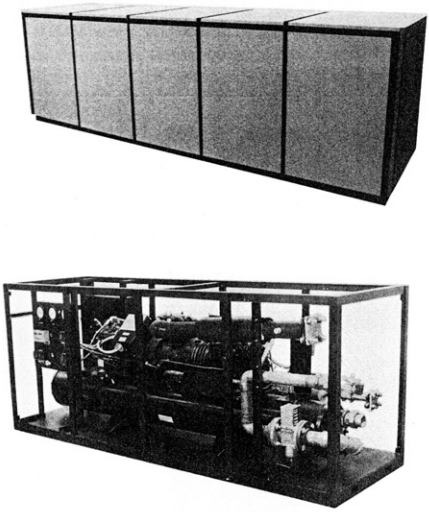

Figure 1-8. Condensing unit

MOTOR-GENERATOR UNITS

Motor-generator units convert primary power from the commercial power mains to the 400 Hz power used by the CRAY-1 Computer System. These units isolate the system from transients and fluctuations on the commercial power mains. The equipment consists of two or three motor-generator units and a control cabinet. Figure 1-10 shows a typical motor-generator and the control cabinet.

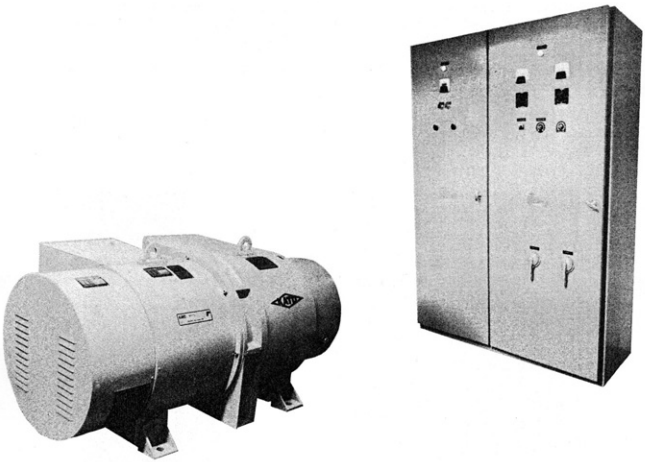

Figure 1-10. Motor-generator equipment

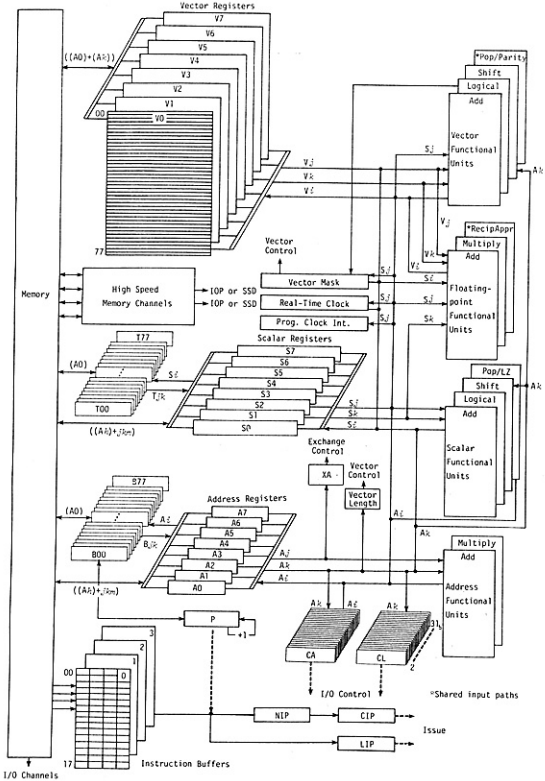

Figure 3-2. Control and data paths in the CPU

CLOCK PERIOD

The basic unit of CPU computation time is 12.5 nanoseconds (ns) and is referred to as a clock period (CP). Instruction issue, memory references, and other timing considerations are often measured in CPs.

MEMORY SECTION

CRAY-1 Central Memory consists of 8 or 16 banks of solid state, random access memory (RAM). Four memory size options are available: 524,288 or 1,048,576 or 2,097,152 or 4,194,304 words. Each word is 72 bits (64 data bits and 8 check bits) with banks independent of each other. Sequentially addressed words reside in sequential banks.

Memory cycle time is 4 CPs (50 ns). Access time, that is, the time required to fetch an operand from memory to an operating register, is 11 CPs (137.5 ns). There is no inherent memory speed degradation for a 16-bank memory of less than 4 million words.

The maximum transfer rate for B, T, and V registers is one word per CP; for A and S registers, it is one word per 2 CPs. Transfer of instructions to instruction buffers occurs at a rate of 16 parcels (four words) per CP.

Central Memory features are summarized below and described in detail in section 4.

- From 0.5M to 4M words of integrated circuit memory
- 64 data bits and 8 error correction bits per word
- 8 or 16 interleaved banks
- 4-CP bank cycle time
- Transfer rate
  - 1 word per CP transfer rate to B, T, and V registers
  - 1 word per 2 CP transfer rate to A and S registers
  - 4 words per CP transfer rate to instruction buffers
- Single error correction/double error detection (SECDED)

CONTROL SECTION

The control section performs all decisions related to instruction issue and coordinates the activities for address, scalar, and vector processing. The control section executes 128 basic instruction codes as 16-bit (1-parcel) or 32-bit (2-parcel) instructions and provides for register reservation, memory field protection, memory access, and interrupt control.

Control section features are summarized below and described in detail in section 5.

- 12.5 nanosecond clock period (CP)
- 4 instruction buffers of 64 16-bit parcels each
- 128 basic instruction codes
- Program exchange mechanism
- Error/monitor interrupt flags
- Memory and program field protection

COMPUTATION SECTION

The computation section contains registers and functional units operating together to execute a program of instructions stored in memory.

Eight address (A) registers store 24-bit integers or addresses. Sixty-four intermediate address (B) registers store data for use by the A registers. Eight scalar (S) registers store 64-bit operands for scalar operations. Sixty-four intermediate (T) registers store data temporarily for the S registers. Eight vector (V) registers, used in vector processing, consist of 64 elements in each register. Each element stores 64-bits.

A vector is an ordered set of elements. A vector instruction operates on a series of elements repeating the same function and producing a series of results. Scalar processing starts an instruction, handles one operand or operand pair, then stops the operation. The main advantage of vector over scalar processing is eliminating instruction start-up time for all but the first operand.

Integer or floating-point arithmetic operations are performed in the computation section. Integer arithmetic is performed in twos complement mode. Floating-point quantities have signed magnitude representation.

Floating-point instructions provide for addition, subtraction, multiplication, and reciprocal approximation. Reciprocal approximation instructions provide for a floating-point divide operation using a multiple instruction sequence. These instructions produce 64-bit results.

Integer or fixed-point operations are integer addition, integer subtraction, and integer multiplication. Integer addition and subtraction operations produce either 24-bit or 64-bit results. An integer multiply operation produces a 24-bit result. A 64-bit integer multiply operation is done through a software algorithm using the Floating-point Multiply functional unit to generate multiple partial products. These products are then shifted and merged to form the full 64-bit product. No integer divide instruction is provided; the operation is accomplished through a software algorithm using floating-point hardware.

The instruction set includes Boolean operations for OR, AND, equivalence, and exclusive OR and for a mask-controlled merge operation. Shift operations allow manipulation of either 64-bit or 128-bit operands to produce 64-bit results. With the exception of 24-bit integer arithmetic, most operations are implemented in vector and scalar instructions. The integer product is a scalar instruction designed for index calculation. Full indexing capability allows the programmer to index throughout memory in either scalar or vector modes. The index can be positive or negative in either mode. Indexing allows matrix operations in vector mode to be performed on rows or the diagonal as well as conventional column-oriented operations.

Population and parity counts are provided for vector and scalar operations. Additionally, scalar operations can include leading zero counts.

Characteristics of the computation section are summarized below and described in detail in section 6.

- Integer and floating-point arithmetic
- Twos complement integer arithmetic
- Signed magnitude floating-point arithmetic
- Address, scalar, and vector processing modes
- Thirteen functional units
- Eight 24-bit address (A) registers
- Sixty-four 24-bit intermediate address (B) registers

- Eight 64-bit scalar (S) registers
- Sixty-four 64-bit intermediate scalar (T) registers
- Eight 64-element vector (V) registers, 64 bits per element

INPUT/OUTPUT SECTION

If a CRAY-1 Computer System uses an I/O Subsystem, a Memory Channel transfers data between Central Memory and the Buffer I/O Processor (BIOP). An optional second Memory Channel transfers data between Central Memory and a Disk I/O Processor (DIOP) or Auxiliary I/O Processor (XIOP). (Software does not currently support data transfers using the Memory Channel to the XIOP.) Each channel is 64 bits wide and uses 8 check bits with each word. Data words are transferred in blocks of 16 under control of Data Ready and Data Transmit control signals. A maximum transfer rate of approximately 850 Mbits per second is possible on the Memory Channel.

Normal input and output communication with the CPU is over 12 full duplex 16-bit channel pairs. Associated with each channel are control lines that indicate data is on the channel.

On the CRAY-1 Computer System, the SSD requires a Memory Channel and a special controller to connect to the mainframe. This linkage also uses one of the 12 standard I/O channel pairs available on the mainframe.

Channel features of the input/output section are summarized below and described in detail in section 7.

- Up to twelve I/O channel pairs; 50 Mbits per second maximum rate
  - Four channel groups containing either 6 input or 6 output channels
  - Channel groups served equally by memory (scans each group every 4 CPs)
  - Channel priority resolved within channel groups
  - 16 data bits, 3 control bits, and 4 parity bits in each direction
  - Lost data detection

Each module has 96 pin pairs for interconnecting to other modules. All interconnections are via twisted pair wire. The average utilization of pins is approximately 60 percent.

Each module has 144 available test points used for trouble shooting. Test points are driven by circuits that do not drive other loads.

CLOCK

All timing within the mainframe is controlled by a single-phase synchronous clock network. This clock has a period of 12.5 nanoseconds. All of the lines that carry the clock signal from the central clock source to the individual modules of the mainframe are of uniform length so that the leading edge of a clock signal arrives at all parts of the mainframe cabinet at the same time. A 3.3-nanosecond pulse (figure B-3) is formed on each module.

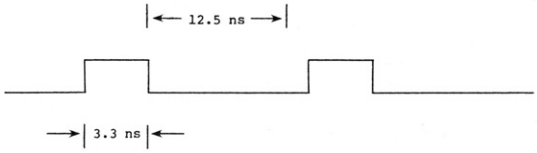

Figure B-3. Clock pulse waveform

POWER SUPPLIES

Thirty-two power supplies are used for the 12-column models, or 20 for the 8-column models. There are 20 -5.2 volt power supplies and 12 -2.0 volt power supplies in the 12-column version. There are 12 -5.2 volt power supplies and 8 -2.0 volt power supplies in the 8-column version. The supplies are divided into 12 or 8 groups, each group supplying one column. A logic column uses one -5.2 volt power supply and one -2.0 volt power supply. A memory column uses two -5.2 volt power supplies and one -2.0 volt power supply. The power supply design assumes a constant load. The power supplies do not have internal regulation but depend on the motor-generator to isolate and regulate incoming power. The power supplies use a 12-phase transformer, silicon diodes, balancing coil, and a filter choke to supply low ripple DC voltages. The entire supply is mounted on a refrigerant-22 cooled heat sink. Power is distributed via bus bars to the load.